**Course Title: Digital Logic and System Design**

**Course Code: CSE 210**

**Credit Hour: 1.5**

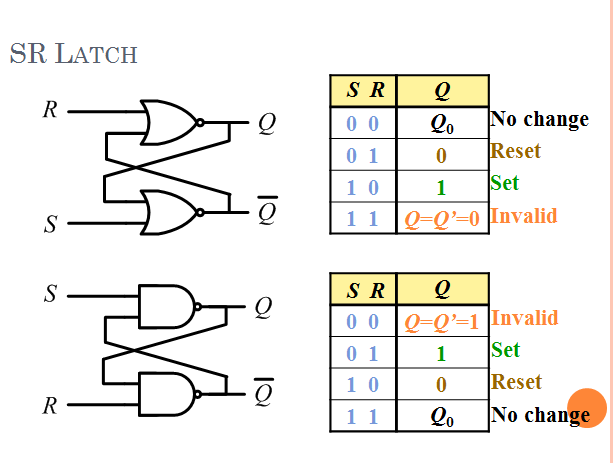
**Experiment No. 5**

**Experiment Name:**

a) Implement and verify SR Latch with NAND and NOR gate.

**Tasks:**

**a) Implement and verify SR Latch with NAND and NOR gate:**



**Report:**

1) Problem Statement

2) Instruments (used in this experiment)

3) Truth Table

4) Logic diagram

5) Discussion